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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,198	11/17/2003	Seung Hee Nam	8733.936.00-US	9565

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EXAMINER	
QI, ZHI QIANG	
ART UNIT	PAPER NUMBER
2871	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,198	NAM ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 31, 2007 has been entered.

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

In claim 1, lines 14-15, recitation ". . .exposing the entire surface of the gate pad and the data pad protection electrode of the pad part by a etching process using the cutting-off plate without forming a photoresist pattern; . . ." is not definite and is not clear. The etching process is dry etching process (see claims 5 and 6). The specification described the dry etching process using photoresist pattern (see paragraph 0101). For examination purpose, it is interpreted as using photoresist pattern.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,380,559 B1 (Park et al) in view of US 6,255,130 B1 (Kim 130), and further in view of US 6,429,057 B1 (Hong et al) and US 5,517,342 (Kim 342).

Regarding claim 1, **Park** teaches (col.6, line 51 – col.13, line 52; Figs.1-5) that a fabrication method of a liquid crystal display panel comprising forming a substrate including a plurality of thin film transistor array, the thin film transistor array having a thin film transistor (TFT 3) at crossings of gate lines (22) and data lines (62) formed on a substrate, a gate pad part including a gate pad (24) connected to the gate line (22) and a data pad part including a data pad (64) connected to the data line (62) and having double layer structure for the pad, so that the date pad (64) having upper layer (642) functions as a data pad protection electrode connected to the data pad (lower layer 641) as shown in Fig.4, wherein the step of forming the thin film transistor array substrate comprises the step of:

- forming gate line assembly (gate pattern) including gate electrode of the thin film transistor, gate line (22) connected to the gate electrode and the gate

pad (24) connected to the gate line (22) (see Fig.2) on the substrate by using mask (see col.2, lines 55-64) that would be by use of a first masking process;

- forming a gate insulation film (30) on the substrate (10) where the gate pattern is formed (see Fig.4);
- forming data line assembly (source/drain pattern) including a source electrode (65) and a drain electrode (66) of the thin film transistor, a data line (62) connected to the source electrode, the data pad (64) connected to the data line (62), a source/drain pattern including a storage capacitors (such as pixel electrode 82 overlapped with gate line 22 as shown in Fig.5), and a semiconductor pattern is formed by etching the passivation layer (see col.2, line 59 – col.3, line 13), i.e., a semiconductor pattern formed in the lower part according to the source/drain pattern on the gate insulating film and such forming process by using second mask that would be by use of a second masking process;
- forming pixel electrode (using ITO transparent conductive electrode) by using mask (see col.3, lines 14-17), and the pixel electrode (82) is connected to the drain electrode (66), and the pixel electrode can be a storage electrode, and such transparent electrode (pixel electrode) pattern including a data pad protection electrode (such as double layered structure 642, 641 for the data pad 64), and such process is formed by mask, and that is by a third masking process;
- forming a passivation layer (70) on the substrate (10).

Park does not explicitly teach:

1) preparing a cutting-off plate having an opening region and a cutting-off region, and arranging the cutting-off plate on the substrate so that the opening region overlaps with the pad part and the cutting-off region overlaps with the remainder part other than the pad part of the substrate (display area) wherein the cutting-off plate of cutting-off region is formed by a metal other than molybdenum, and exposing the entire surface of the gate pad of the pad part and the data pad protection electrode (peripheral area) by a etching process using the cutting-off plate and using a photoresist pattern;

2) forming entirely a protection film on the substrate after the transparent electrode pattern forming process.

Park further teaches (col.10, line 26 –col.12, line 67; Figs.9-12) that the etching process using mask (such as mask 300 and 400), and generally, the mask process includes preparing a mask, and that is conventional as first preparing a mask and then using such mask process (see applicant's Remark filed on July 13, 2007, page 5, lines 8-12 for the explanation of the mask process).

The function of the cutting-off plate is the same as the function of a mask (this invention is to use a cutting-off plate as a mask), because the cutting-off plate having open portion (open region) and opaque portion (cutting-off region) that allows the light passing through the open portion; and using mask to expose the gate pad and the data pad of the pad part by etching process using a mask, and arranging a mask on a region

to form the pad part, so that the opaque portion (cutting-off region) is on a region of the substrate other than the region of the pad part, and inherently, the open region overlaps with the pad part and the cutting-off region overlaps with the region other than the pad part .

Park further teaches (col.10, lines 28-45) that the light exposure at the display area D is different from the light exposure at the peripheral area P, such that the molecules at the display area and at the peripheral area being resolved by using mask to a predetermined depth from the surface.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the fabrication method of a liquid crystal display panel of Park with the teachings of preparing and arranging a mask (cutting-off plate) and exposing the gate pad and the data pad protection electrode by etching process using the mask (cutting-off plate) as taught by Park, since the skilled in the art would be motivated for obtaining the molecules at the display area and at the peripheral area being resolved by using mask to a predetermined depth from the surface (col.10, lines 28-45).

Concerning the cutting-off plate of cutting-off region is formed by a metal other than molybdenum, **Kim 130** teaches (col.9, lines 49-63; Fig.7B) that a photomask (400) having a plurality of slits (410) (open portion), and a metal Cr layer is coated on the mask (400) to reduce the amount of exposing light.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the fabrication method of a liquid crystal display panel of

Park with the teachings of using a metal cutting-off plate as taught by Kim 130, since the skilled in the art would be motivated for achieving efficiently shield the light exposing in the opaque portion (cutting-off region) of the cutting-off plate.

Concerning the difference of the steps order wherein forming a protection film on the substrate after the transparent electrode pattern forming process, **Hong** further teaches (col.2, lines 5-23) that a method of manufacturing thin film transistor array in which forming a gate wire using first photolithography process, forming a data conductor layer using a second photolithography process, forming a conductive pattern (pixel electrode pattern) using a third photolithography process, and finally a passivation layer (a protection film) is formed, such that the step of forming entirely a protection film on the substrate after forming the transparent electrode (pixel electrode) pattern. Hong further teaches (col.1, lines 9-11) that such manufacturing method would reduce the number of manufacturing steps.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the fabrication method of a liquid crystal display panel of Park and Kim 130 with the teachings of forming a passivation layer after forming the pixel electrode pattern as taught by Hong, since the skilled in the art would be motivated for reducing the number manufacturing steps.

Concerning forming entirely a protection film on the substrate that would be without the necessary to use mask as the entire surface would be the protection film, and inherently, simplifying the manufacturing process.

As evidence, **Kim 342** teaches (col. 10, lines 51-52) that a protective layer covers the inner surface of the rear substrate, and further teaches (col.18, lines 34-35; Fig.13) that a protective layer (6) is formed on the whole surface of the substrate. Therefore, such protection film entirely formed on the substrate would protect all the components and signal lines on the substrate, and inherently without necessitating the use of a masking process as the protective film entirely formed on the substrate.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the fabrication method of a liquid crystal display panel of Park and Hong with the teachings of forming entirely a protection film on the substrate as taught by Kim, since the skilled in the art would be motivated for achieving more protection for all the components on the substrate.

Regarding claim 2, Park teaches (col.1, lines 13-24) that generally, liquid crystal display is formed with two glass substrates (TFT array substrate and color filter substrate) and need to be assembled, and the forming method performing photolithography by using mask. Such that the gate pad and the data pad electrode are exposed, and that is a general manufacturing method, and that would have been at least obvious.

Regarding claims 5 and 6, Park teaches (col.3, lines 29-30) that the etching for forming the gate pad and data pad being performed by using dry etching, and inherently, removing insulating layer and gate insulating part formed in the gate pad part and removing insulating film formed on the data pad part and the gate insulating film not

overlapped with the data pad protection electrode so as to obtain a desired pads arrangement for the thin film transistor panel, and that would have been obvious.

Response to Arguments

5. Applicant's arguments with respect to claims 1-2 and 5-6 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the data pad directly contacts with the data pad protection electrode without contact hole and the gate pad and the data pad protection contact the TCP without contact hole) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Concerning the data pad directly contacts with the data pad protection electrode without contact hole and the gate pad and the data pad protection contact the TCP without contact hole, a prior art of record such as US 5,744,821 (Song) teaches (Fig.3) that pixel electrode (111) directly contact the drain electrode (110) that is same principle to connect the pads with the data pad protection electrode or the TCP, and inherently, would prevent the contact failure, and that would have been obvious.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 7:30 am-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mike Qi
Primary examiner
Nov. 21, 2007